**IN THE CLAIMS**

1. (currently amended) A data processing apparatus adapted for performing scramble processing of transmit data, the data processing apparatus comprising:

scramble operation processing means including plural stages of shift registers, and a cyclic operation processing circuit for performing a predetermined operation processing on the basis of a hold value of a predetermined stage of the shift registers and the transmit data to generate scramble-processed data~~, and to sequentially input the scramble processed data to the input stage of the shift register~~;

data generating means for generating bit data of a predetermined pattern and for supplying the generated bit data of the predetermined pattern to one or more of the shift registers and for outputting same; and

switching means supplied with the scramble-processed data and the bit data of the predetermined pattern generated by the data generating means to select the bit data of the predetermined pattern at the time of synchronization processing of transmit data, and to select the scramble-processed data when synchronization processing of transmit data is not performed to output the data thus selected as scrambler output data.

2. (currently amended) The data processing apparatus as set forth in claim 1,

wherein the data generating means is caused to be of the configuration to load the bit data of the predetermined pattern into ~~the~~ at least one shift register at the time of synchronization processing of transmit data.

3. (original) The data processing apparatus as set forth in claim 1 or 2,

wherein the switching means is caused to be of the configuration in which in the case where a predetermined synchronization pattern data inserted into the transmit data for the purpose of taking synchronization of the transmit data is inserted in the transmit data, the switching means serves to select the bit data of the predetermined pattern to output the bit data thus selected as scrambler output data.

4. (original) The data processing apparatus as set forth in claim 1,

wherein the data generating means is caused to be of the configuration to generate bit data of a predetermined pattern to which predetermined information is assigned in advance.

5. (currently amended) A data processing apparatus adapted for performing scramble processing of transmit data, the data processing apparatus comprising:

cyclic code generating means for generating cyclic bit data train of a predetermined period;

EXOR operation means for sequentially performing EXOR operation of the cyclic bit data train with respect to the transmit data to output scramble-processed data;

data generating means for generating bit data of a predetermined pattern and for supplying the generated bit data of the predetermined pattern to the cyclic code generating means and for outputting same; and

switching means supplied with the scramble-processed data and bit data of a predetermined pattern generated by the data generating means to select the bit data of the predetermined pattern at the time of synchronization processing of transmit data, and to select the scramble-processed data when synchronization processing of the transmit data is not performed to output the data thus selected as scrambler output data.

6. (original) The data processing apparatus as set forth in claim 5,

wherein the switching means is caused to be of the configuration in which in the case where a predetermined synchronization pattern data inserted into the transmit data for the purpose of taking synchronization of the transmit data is inserted in the transmit data, the switching means serves to select the bit data of the predetermined pattern to output the bit data thus selected as scrambler output data.

7. (original) The data processing apparatus as set forth in claim 5,

wherein the data generating means is caused to be of the configuration to generate bit data of a predetermined pattern to which predetermined information is assigned in advance.

8. (canceled)

9. (canceled)

10. (new) A data processing apparatus adapted for performing scramble processing of transmit data, the data processing apparatus comprising:

a random number generating circuit to generate a random bit data train, said random number generating circuit having a first shift register, a second shift register, and a first adder, said random number generating circuit being arranged such that (i) an output stage of the first shift register is coupled to an input stage of the second shift register and to the first adder, and (ii) an output stage of the second shift register is coupled to the first adder;

a data generator to generate bit data of a predetermined pattern and to supply the generated bit data of the predetermined pattern therefrom;

a second adder arranged to receive an output of the first adder and the transmit data and being operable to generate scramble-processed data therefrom;

a first switch arranged to receive the scramble-processed data and the bit data of the predetermined pattern, said first switch being operable to select the bit data of the predetermined pattern at the time of synchronization processing of the transmit data and to select the scramble-processed data when synchronization processing of the transmit data is not performed and to output the data selected.

11. (new) The data processing apparatus according to claim 10, in which the data generator is further arranged to supply the generated bit data of the predetermined pattern to the first shift register and the second shift register, and in which said random number generating circuit is further arranged such that the output of the first adder is supplied to an input stage of the first shift register.

12. (new) The data processing apparatus according to claim 11, in which the first adder is a modulo 2 adder, and in which the first adder and the second adder are each operable to perform an exclusive-or operation.

13. (new) The data processing apparatus according to claim 10, further comprising a second switch arranged to receive the output of the first adder and the bit data of the predetermined pattern and being operable to output a selected one of the output of the first adder and the bit data of the

predetermined pattern to an input stage of the first shift register.

14. (new) The data processing apparatus according to claim 13, in which the first adder is a modulo 2 adder, and in which the first adder and the second adder are each operable to perform an exclusive-or operation.